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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,976	NOE, AMANDA	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13,18,20,21 and 23-27* is/are rejected.

7)☒ Claim(s) *10-12,14-17,19 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 December 2006 has been entered.

Status of Claims

2. Claims 1-27 are pending in the Application.

Claims 1, 8 and 24 have been amended.

Claims 1-9, 13, 18, 20-21 and 23-27 are rejected.

Claims 10-12, 14-17, 19 and 22 are objected to.

Response to Amendment

3. Applicant's amendments and arguments filed on 28 December 2006 in response to the office action mailed on 6 September 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-8, 18, 20 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg (US PG Publication 2002/0159483 A1) in view of Craft (US Patent 5,652,878), and in further view of Agrawal et al. (US Patent 6,919,736 B1), hereinafter Agrawal.

As for claim 1, Clauberg teaches a method comprising:

receiving a serial stream of data bits (paragraph 0023, lines 1-8 – the system can receive unaligned parallel or serial bits);

deserializing the serial stream of data bits into parallel bits (paragraph 0024, lines 1-3 - data is transformed into parallel bits);

inputting the parallel bits into a first register (Fig. 2, the deserializer feeds the parallel data into a register (element 214) via the demux (element 212) – paragraph 0032, lines 1-17);

inputting an output of the first register to a second register (Fig. 2, element 216 – the shift register receives the data from the first register (element 214) – paragraph 0032, lines 1-17);

inputting outputs of the first and second resisters to a memory, wherein the parallel bits, output of the first register, and output of the second register are

combined and stored as a first parallel word in a memory (Fig. 2, element 216 – the shift register receives the data from the first register (element 214) – paragraph 0032, lines 1-17). Note in Fig. 2, the 16-bit parallel output (212) is used to generate 4 16-bit outputs from the first register (212), which is sent to a second register (214). In other words, the output depicted by Fig. 2, element 204 is a combination of inputted parallel bits, which are used as an input to a first register, whose output is fed into a second register (i.e. the parallel bits are combined with two outputs of the registers before being outputted to the memory).;

providing the parallel bits in a plurality of parallel bit output formats (The parallel output from the demux is fed into the shift register (Fig. 2, element 216). The shift register is capable of shifting the outputted data into any of the a plurality of parallel formats (i.e. the bit at position 1 can be shifted to any of the other 7 positions. Clauberg exploits this shifting pattern in order to align the position of the outputted bits – paragraph 0032, lines 1-17);

Though Clauberg teaches outputting the data from the first two registers (data stored in register (element 214) is sent to the shift register (element 216) which is eventually outputted (element 204)) into a storage unit, (abstract, lines 5-8 – a storage unit stores data from the outgoing data stream), and though it is well known in that art that Clauberg could use any sort of common memory to store his outgoing data (i.e. a RAM), he still fails to teach or suggest specifically using a CAM. Additionally he fails to teach storing the parallel output of the shift register as parallel words in the content

addressable memory, wherein at least one of the set of parallel words includes a fixed frame alignment detection pattern having a data position and simultaneously comparing the first parallel word to the set of parallel words stored in the content addressable memory to detect a frame alignment pattern within the first parallel word.

Craft however teaches a method and apparatus of compressing data, which includes a circuit for storing incoming data (col. 2, lines 59-63). More specifically, Craft teaches implementing his circuit by use of a CAM rather than a RAM (col. 3, lines 42-50).

Craft further teaches a method and apparatus of compressing data, which includes a circuit for storing incoming data (col. 2, lines 59-63). More specifically, Craft teaches implementing his circuit by use of a CAM rather than a RAM (col. 3, lines 42-50). Additionally, note Craft specifically teaches simultaneously comparing the newly stored incoming word with data previously stored within the other entries of the cache to determine if a match occurs (col. 2, line 59 through col. 3, line 8). It is additionally worthy to note that this sort of storing and comparing is common to CAM memories in general. Also note, since the data outputted by Clauberg's system is of a particular type and alignment, each newly stored set of data in the CAM would be compared with other aligned data with fixed patterns and respective positions within the word received from Clauberg's frame byte alignment unit.

Craft further teaches selecting one of the parallel bit output formats to output based on match flag outputs from the CAM once a particular frame alignment pattern is detected, wherein each of the match flag outputs are associated with a respective one

of the set of parallel words that includes the matching frame alignment pattern and the matching data position with respect to the frame alignment pattern on the first parallel word (col. 5, lines 1-9 – a plurality of entries are stored in the CAM array, match flag signals (342) are generated based on the comparison of the data stored in the CAM with the data in the input buffer).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to store his outputted parallel data into the CAM as taught by Craft, rather than a standard means, such as with a random access memory. By doing so, Clauberg would benefit by improving the compressing ratio of the stored data, and increase throughput during transmission of the data as taught by Craft in col. 3, lines 50-57.

Additionally, though the combined teaching of Clauberg and Craft disclose providing a bus configured to receive the parallel bits and output of the first register (Clauberg – Fig. 2 (output bus)), they fail to teach the data lines forming that bus as being grouped into a plurality of overlapping subsets of the bus, each containing at least one common data line as recited in the claim.

Agrawal however teaches an FPGA device having embedded memory with configurable depth and width in which he discloses overlapping the bits of the configurable memory block on a common shared interconnect bus (see the abstract and col. 12, lines 45-53 – the bits of the wide words of each memory block share interconnect buses on a overlapping basis)

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to further include Agrawal's FPGA device with configurable memory into his own frame byte alignment unit. By doing so, Clauberg's system would benefit by having a more versatile and efficient storage unit for storing data from his output data stream. This memory would be capable of concatenating memory partitions, which would otherwise operate independently as taught by Agrawal in col. 3, lines 14-37. Additionally, Clauberg could benefit by exploiting the advantages of using Agrawal's memory as either a FIFO or LIFO device for data streams which is extremely beneficial to speed critical data as taught by Agrawal in col. 2, lines 49-64.

As for claim 24, Clauberg teaches a method comprising:

deserializing an input serial data stream into a first parallel word (paragraph 0024, lines 1-3 - data is transformed into parallel bits);;

generating a second parallel word from the first parallel word stored (Fig. 2, the 16-bit serial data is sent to a demux (Fig. 2 (2112)) which generates 4 separate 16-bit words, any of which may be considered to a second parallel word. For the purposes of applying art, two of the 16-bit words will be considered the second parallel word);

grouping the second parallel word into a plurality of data word subsets (Fig. 2, the second word contains two sets of words (two 16-bit words);

generating a third parallel word from the combination of the first and second parallel word, wherein the third parallel word is wider than the first parallel word and the second parallel word (the output (third parallel word –

element 204) consists of a 64-bit which was comprised in part by the combination of the first and second words); and

detecting a frame alignment symbol within the third parallel word by comparing a bit pattern of the third parallel word to a plurality of frame alignment patterns stored in a memory (the alignment position (i.e. symbol) is contained in the 192-bit portion of the data stream, which is subsequently sent to the extracting unit (paragraph 0027, all lines).

Though Clauberg teaches comparing a bit pattern of the third parallel word to a plurality of frame alignment patterns stored in a memory, he fails to teach the memory as being specifically a CAM. Though it is well known in that art that Clauberg could use any sort of common memory to store and compare his outgoing data (i.e. a RAM), he still fails to teach or suggest specifically using a CAM. Additionally, Clauberg teaches each of the fixed frame alignment patterns as being part of a respective one of a set of parallel words (Clauberg specifically teaches aligning parallel data in accordance to specific patterns/protocols).

Craft however teaches a method and apparatus of compressing data, which includes a circuit for storing incoming data (col. 2, lines 59-63). More specifically, Craft teaches implementing his circuit by use of a CAM rather than a RAM (col. 3, lines 42-50).

Craft further teaches selecting one of the parallel bit output formats to output based on match flag outputs from the CAM (i.e. comparison to fixed frame alignment patterns), wherein the match flag outputs are generated in response to the inputs to the

CAM (col. 5, lines 1-9 – a plurality of entries are stored in the CAM array, match flag signals (342) are generated based on the comparison of the data stored in the CAM with the data in the input buffer).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to store his outputted parallel data into the CAM as taught by Craft, rather than a standard means, such as with a random access memory. By doing so, Clauberg would benefit by improving the compressing ratio of the stored data, and increase throughput during transmission of the data as taught by Craft in col. 3, lines 50-57.

Additionally, though the combined teaching of Clauberg and Craft disclose grouping the second parallel word into a plurality of subsets, they fail to teach the data lines forming that bus as being grouped into a plurality of overlapping subsets of the bus, each containing at least one common data line as recited in the claim.

Agrawal however teaches an FPGA device having embedded memory with configurable depth and width in which he discloses overlapping the bits of the configurable memory block on a common shared interconnect bus (see the abstract and col. 12, lines 45-53 – the bits of the wide words of each memory block share interconnect buses on a overlapping basis)

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to further include Agrawal's FPGA device with configurable memory into his own frame byte alignment unit. By doing so, Clauberg's system would benefit by having a more versatile and efficient storage unit for storing data from his

output data stream. This memory would be capable of concatenating memory partitions, which would otherwise operate independently as taught by Agrawal in col. 3, lines 14-37. Additionally, Clauberg could benefit by exploiting the advantages of using Agrawal's memory as either a FIFO or LIFO device for data streams which is extremely beneficial to speed critical data as taught by Agrawal in col. 2, lines 49-64.

As for claim 25, Clauberg teaches selecting one of the subsets associated with a respective one of the frame alignment patterns that match the frame alignment symbol (paragraph 0028 – all lines. Sequence is output once alignment is identified).

As for claim 26, Clauberg teaches detecting the frame alignment symbol within one clock cycle (paragraph 0028, all lines. Clauberg teaches locating the alignment within one cycle).

As for claim 27, though Clauberg teaches grouping the second parallel word as comprising outputting the second parallel word, he fails to teach grouping them on a data bus that includes subsets of data lines that correspond to the data word subsets.

Agrawal however teaches an FPGA device having embedded memory with configurable depth and width in which he discloses overlapping the bits of the configurable memory block on a common shared interconnect bus corresponding to data word subsets (see the abstract and col. 12, lines 45-53 – the bits of the wide words of each memory block share interconnect buses on a overlapping basis)

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to further include Agrawal's FPGA device with configurable memory into his own frame byte alignment unit. By doing so, Clauberg's system would

benefit by having a more versatile and efficient storage unit for storing data from his output data stream. This memory would be capable of concatenating memory partitions, which would otherwise operate independently as taught by Agrawal in col. 3, lines 14-37. Additionally, Clauberg could benefit by exploiting the advantages of using Agrawal's memory as either a FIFO or LIFO device for data streams which is extremely beneficial to speed critical data as taught by Agrawal in col. 2, lines 49-64.

As for claim 3, Clauberg teaches the 8 parallel bits (referring paragraph 0024, lines 7-11, the incoming data stream can be either 2, 4, 8, 16 etc. bits. The deserializer would then take the incoming serial bits and convert them to 8, 16, 32, or 64 bits wide respectively as indicated in paragraph 0025, lines 1-5).

As for claim 4, Clauberg teaches the first and second registers as being two stages of a shift register (referring to Fig.2, the two registers (214) and (216) work in tandem to shift the data outputted from the demux hence are two stages of a shift register).

As for claim 5, Craft teaches the depth of the CAM comprising at least one row for each of the parallel bits (col. 6, line 65 through col. 7, line 7 – the CAM array can be 1,012 sections deep. Note Clauberg teaches a taking a 16-bit serial input to generate a 64-bit parallel output in paragraph 0025, lines 1-5).

As for claim 6, Clauberg teaches the inputs of the CAM as being provided by way of parallel transfer (the deserialized data is outputted to storage (i.e. Craft's CAM) via the output port (Fig. 2, element 204)).

As for claim 7, Clauberg teaches the width of the parallel bits input into the CAM as being at least a number of parallel bits output from the deserializer plus a length of a pattern to be detected using the CAM minus 1 (using the example of 64 bits being output from his deserializer (Clauberg, paragraph 0025, lines 1-5 – the output is fed to the CAM via the output (Fig. 2, element 204). The 64 bits are then transmitted to the CAM. These bits are then compared to the word in the input data buffer of the CAM (i.e., the pattern to be detected – Craft, col. 5, lines 1-9). Though the word size is not specifically set forth by Craft, it is well know in the art that a word is 16 bits in length.

As for claim 8, Clauberg teaches a circuit comprising:

a deserializer circuit coupled to receive serial data input and outputting a first parallel data of output (Fig. 2, element 206 – paragraph 0031, lines 1-2); and

a shift register coupled to the first parallel data output (Fig. 2, element 216 – paragraph 32, lines 1-9);

Further, though it is well known in that art that Clauberg could use any sort of common memory to store his outgoing data - (abstract, lines 5-8 – a storage unit stores data from the outgoing data stream - i.e. a RAM), he still fails to teach storing the parallel output of the shift register as a first parallel word in a first row of the content addressable memory that is simultaneously compared to a set of parallel words employed by the content addressable memory to detect a pattern within the first parallel word, wherein each parallel word of the set of parallel words includes a fixed data pattern to detect the pattern in the first parallel word, wherein each fixed data pattern

includes a respective data position within a respective data word as recited in the instant claim.

Craft however teaches a method and apparatus of compressing data, which includes a circuit for storing incoming data (col. 2, lines 59-63). More specifically, Craft teaches implementing his circuit by use of a CAM rather than a RAM (col. 3, lines 42-50). Additionally, note Craft specifically teaches simultaneously comparing the newly stored incoming word with data previously stored within the other entries of the cache to determine if a match occurs (col. 2, line 59 through col. 3, line 8). It is additionally worthy to note that this sort of storing and comparing is common to CAM memories in general. Also note, since the data outputted by Clauberg's system is of a particular type and alignment, each newly stored set of data in the CAM would be compared with other aligned data with fixed patterns and respective positions within the word received from Clauberg's frame byte alignment unit.

Additionally, though the combined teaching of Clauberg and Craft disclose providing a bus configured to receive the parallel bits and using a deserializer to output the data (Clauberg – Fig. 2 (output bus)), they fail to teach the data lines forming that bus as being grouped into a plurality of overlapping subsets of the bus that each contain at least one common data line as recited in the claim.

Agrawal however teaches an FPGA device having embedded memory with configurable depth and width in which he discloses overlapping the bits of the configurable memory block on a common shared interconnect bus (see the abstract and

col. 12, lines 45-53 – the bits of the wide words of each memory block share interconnect buses on a overlapping basis)

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to further include Agrawal's FPGA device with configurable memory into his own frame byte alignment unit. By doing so, Clauberg's system would benefit by having a more versatile and efficient storage unit for storing data from his output data stream, capable of concatenating memory partitions, which would otherwise operate independently as taught by Agrawal in col. 3, lines 14-37. Additionally, Clauberg could benefit by exploiting the advantages of using Agrawal's memory as either a FIFO or LIFO device for data streams in a speed-critical path as taught by Agrawal in col. 2, lines 49-64. As for claim 18, Craft teaches the circuit of claim 8 wherein the CAM has a number of rows equal to or greater than a number of bits of the first parallel data output (col. 6, line 65 through col. 7, line 7 – the CAM array can be 1,012 sections deep. Note Clauberg teaches a taking a 16-bit serial input to generate a 64-bit parallel output in paragraph 0025, lines 1-5).

As for claim 20, Clauberg teaches the circuit of claim 8 wherein the first parallel data output is 8, 16, or 32, etc. bits wide (referring paragraph 0024, lines 7-11, the incoming data stream can be either 2, 4, 8, 16 etc. bits. The deserializer would then take the incoming serial bits and convert them to 8, 16, 32, or 64 bits wide respectively as indicated in paragraph 0025, lines 1-5).

As for claim 23, Clauberg teaches the circuit of claim 8, wherein the first parallel data output comprises 8 bits (again referring to paragraph 0024, lines 7-11, the

incoming data stream can be 2 bits, producing a 8-bit parallel output via the 1:4 demultiplexer). The parallel output from the demux is then fed into the shift register (Fig. 2, element 216). The shift register is capable of shifting the outputted data into any of the eight claimed formats (i.e. the bit at position 1 can be shifted to any of the other 7 positions. Likewise each of corresponding remaining seven bits would shift relative to the first. Clauberg exploits this shifting pattern in order to align the position of the outputted bits – paragraph 0032, lines 1-17).

Again, it would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to store his outputted parallel data into the CAM as taught by Craft, rather than a standard means, such as with a random access memory. By doing so, Clauberg would benefit by improving the compressing ratio of the stored data, and increase throughput during transmission of the data as taught by Craft in col. 3, lines 50-57.

5. Claims 2, 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg (US PG Publication 2002/0159483 A1), Craft (US Patent 5,652,878), and Agrawal (US Patent 6,919,736) as applied to claims 1 and 8 above, and in further view of Morikawa (US Patent 6,7470,886).

As for claim 2, though the combined teachings of Clauberg, Craft and Agrawal fail to teach outputting both the parallel bits and the output of the first register into a plurality of tristate driver circuits, Morikawa teaches a content addressable memory with shifted enable signal which includes an input-output circuit which includes tristate buffers (ND1, ND2) – col. 3, lines 43-54. In his disclosure, Morikawa teaches inputting

data outputted from cells the CAM (Fig. 3, element 2) into the input-output circuit (Fig. 3, element 10), which is comprised of a plurality of tristate buffer drivers circuits. Data is the selected via the input-output circuit and outputted as the data output signal DOUT – col. 3, lines 43-54). This selection occurs based on the RWN control signal which enables ND2 to output the signal.

As for claim 9, though the combined teachings of Clauberg, Craft and Agrawal teach a plurality of parallel data output formats based on the first parallel data output, wherein each of second parallel data outputs are associated with a respective one of the subsets, they fail coupling a plurality of tristate buffer circuits to each of the parallel data outputs. Morikawa however teaches a content addressable memory with shifted enable signal, which includes an input-output circuit, including tristate buffers (ND1, ND2) – col. 3, lines 43-54. In his disclosure, Morikawa teaches inputting data outputted from cells the CAM (Fig. 3, element 2) into the input-output circuit (Fig. 3, element 10), which is comprised of a plurality of tristate buffer drivers circuits.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to include Morikawa's CAM with shifted enable signal to his system byte alignment unit. By doing so, Clauberg would benefit from Morikawa's shifting in logic level of the enable signal of his memory which in turn would help to reduce the current consumption of the memory cell, and speed up read/write access of the memory as taught by Morikawa in col. lines 8-13.

As for claim 13, Clauberg teaches one parallel data output format for each bit of the first parallel data output minus 1 (assuming the first parallel output consists of 8 bits

(i.e. 2 bit input to the 1:4 demux – paragraph 0024, lines 7-11), Clauberg teaches at least seven more possible parallel data outputs (i.e. 16, 32, 64, ..., 1024 bits).

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg (US PG Publication 2002/0159483 A1), Craft (US Patent 5,652,878), and Agrawal (US Patent 6,919,736) as applied to claim 8 above, and in further view of Veenstra et al., hereinafter Veenstra (US Patent 6,160,419).

Though the combined teachings of Clauberg, Craft and Agrawal include a circuit including a CAM, a shift register, and a deserializer as claimed by Applicant in claim 8, they fail to disclose making use the circuit in a programmable logic IC implementation as claimed by Applicant.

Veenstra however teaches a programmable logic architecture incorporating a content addressable embedded array block. In his disclosure, Veenstra teaches a programmable IC which is configured to operate as CAM (col. 2, lines 52-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg in further view of Craft to implement his byte alignment unit on the field programmable logic device as taught by Veenstra. By doing so, Clauberg would be able to exploit the benefits of post-manufacturing customization of the circuit as taught by Veenstra in col. 1, lines 26-43).

Response to Arguments

7. Applicant's arguments with respect to the rejections set forth under 35 USC § 103 as applied to claims 1, 8, and 24 have been but are they are not persuasive.

As for these claims, Applicant provides a general overview of the newly added claimed subject matter, and makes a general assertion that Clauberg, Craft, Agrawal, Morikawa and Veenstra, alone or in combination, fail to disclose these claimed elements (see pages 9-10 of Applicant's remarks). Applicant continues on page 10 by describing Clauberg's disclosure, and further asserts "Clauberg does not disclose how the align position detection unit operates".

This argument however is not persuasive, as Applicant failed to show how this alleged deficiency renders the instant claims non-obvious in view of Clauberg, Craft and Agrawal's combined teachings, in order to sufficiently rebut Examiner's previously asserted *prima facia* case of obviousness.

Applicant additionally asserts that Clauberg and Craft are not properly combinable by alleging "Craft's configuration would defeat Clauberg's attempt to generate an aligned data stream having a predetermined width as the token generated would combine data in a compressed form removing the alignment position characteristic and requiring an additional decompression step not disclosed by Clauberg nor Craft to generate the aligned data stream".

This argument however is not persuasive, as Examiner maintains that it would have been obvious for Clauberg to store the aligned data output into the CAM memory as described by Craft. By doing so, Clauberg would benefit by improving the

compressing ratio of the stored data, and increase throughput during transmission of the data as taught by Craft in col. 3, lines 50-57. The compression itself would not remove the alignment undertaken by Clauberg's system, but would rather merely store each subsequently compared and stored entry sequentially as per Clauberg in col. 2, line 59 through col. 3, line 8.

Applicant additionally describes Morikawa and Veenstra disclosures on page 11 of the remarks, however does not distinguish them with the instant claims. These remarks cannot be construed as an argument, hence the comments do not persuade Examiner to remove the rejections.

Applicant lastly asserts, "Agrawal teaches away from a bus having subsets that share a common data line as each of the subsets are mutually exclusive (i.e., they do not share a common data line), the overlap refers to a mode (i.e., shallow-and-wide mode) where a data bus is used to support a single wide word that does not use subsets (see Agrawal Abstract, col. 12 lines 19-28)." Applicant concludes, "[t]herefore, Agrawal is not properly combinable with the cited references. Even if Agrawal could be combined, in the mode where subsets are used in Agrawal (i.e., the deep-and-narrow mode), they do not share a common data line which would defeat the purpose of having subsets of a bus that share a common data line."

This argument however is not persuasive. Examiner maintains that Agrawal does in fact teach shared bus lines for data on overlapping basis, "when the shallow-and-wide mode is invoked, the bits of the wide words of CMB's in alternate columns shared interconnect buses **on an overlapping basis**" (emphasis added) – see abstract

and col. 12, lines 45-53. Clauberg specifically teaches transferring parallel data (closely akin to narrow-and-wide, rather than the shallow-and-deep mode taught by Agrawal), therefore Clauberg would be able to utilize the shallow-and-wide configuration by utilizing multiple overlapping subsets with at least one common data line to transfer the data within his system. Not only are these two references combinable notwithstanding Applicant's assertion to the contrary, Clauberg would be motivated to utilize Agrawal's teachings in that Clauberg's system would benefit by having a more versatile and efficient storage unit for storing data from his output data stream. This memory would be capable of concatenating memory partitions, which would otherwise operate independently as taught by Agrawal in col. 3, lines 14-37. Additionally, Clauberg could benefit by exploiting the advantages of using Agrawal's memory as either a FIFO or LIFO device for data streams which is extremely beneficial to speed critical data as taught by Agrawal in col. 2, lines 49-64.

Applicant's assertion that claims 2-7, 9-23 and 25-27 are allowable for at least further limiting an allegedly allowable respective base claim is rendered moot in view of the rejections and arguments discussed *supra*.

Allowable Subject Matter

8. Claims 10-12, 14-17, 19 and 22 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
4-11-07